ABSTRACT OF THE DISCLOSURE

A device asserts a first wired OR signal line to a low level. This asserted state is transferred to a second system via a first mask mechanism. The second assert mechanism asserts a second wired OR signal line. This asserted state is similarly communicated to a first assert mechanism to maintain the signal line in an asserted state. The device that has made the assertion is processed. Then, values in a first and second registers are changed to negate outputs from the first and a second mask mechanisms. It is verified that the first and second wired OR signal lines have been brought into a negate state. The values in the first and second registers are returned to the initial ones. A switching operation is performed so that each of the first and second mask mechanisms output the state of the wired OR signal line, to return to the initial state.